

09840724-042301

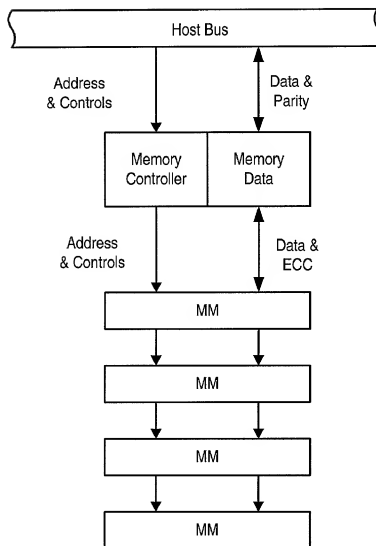


Figure 1
Prior Art

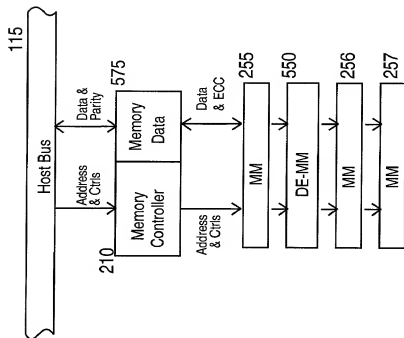
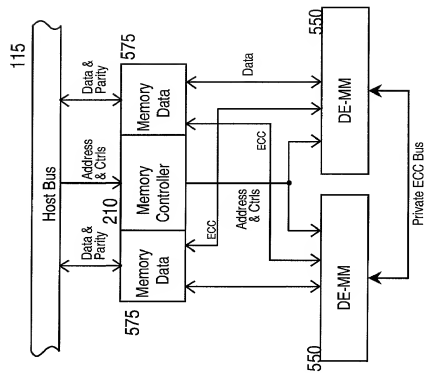


Figure 2a



060402b-042007

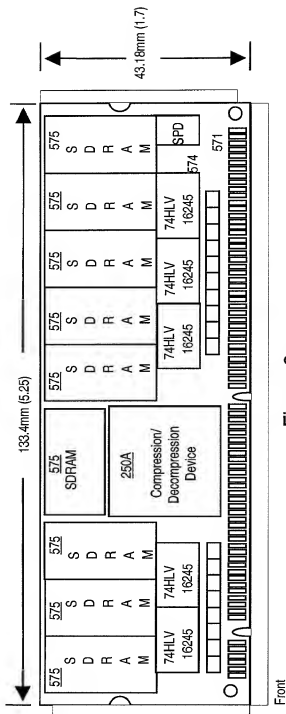


Figure 3a

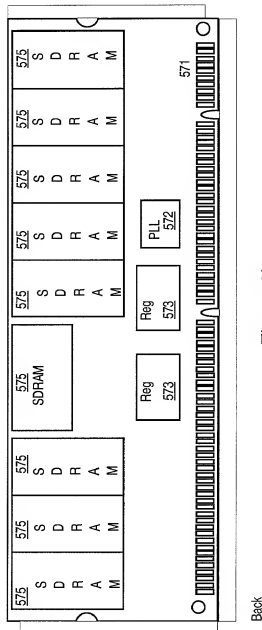


Figure 3b

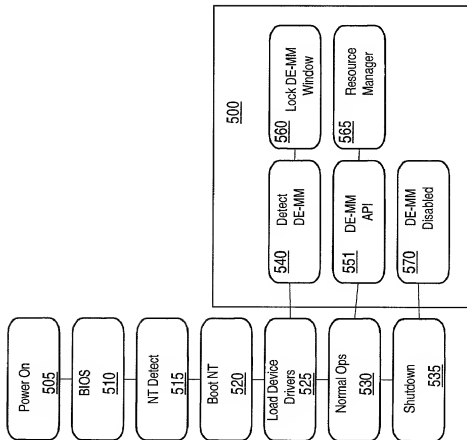


Figure 5

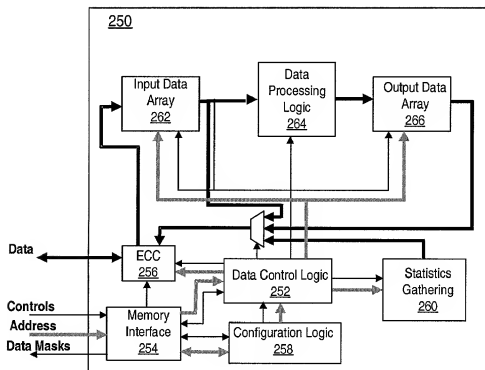


Figure 6

DE-MM device logic

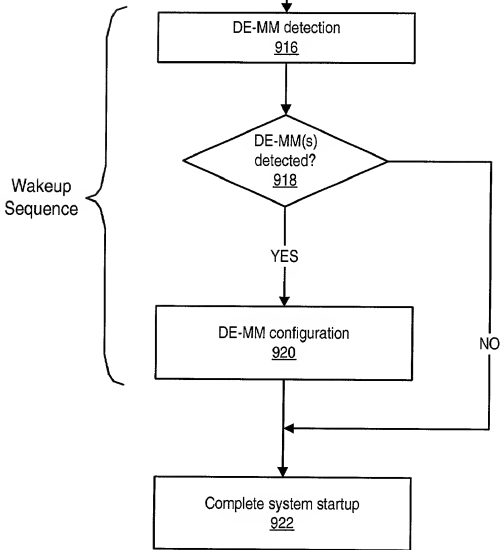


Figure 7a

00000000.00000000

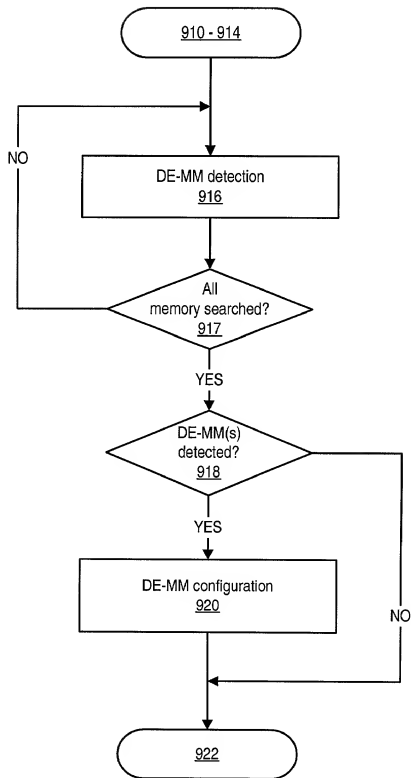


Figure 7b

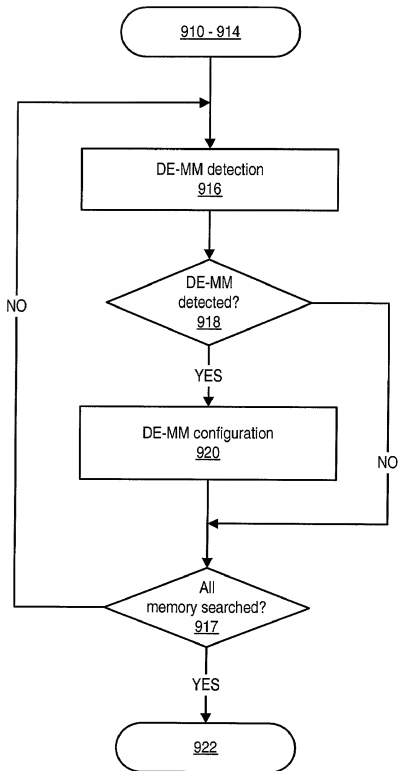


Figure 7c

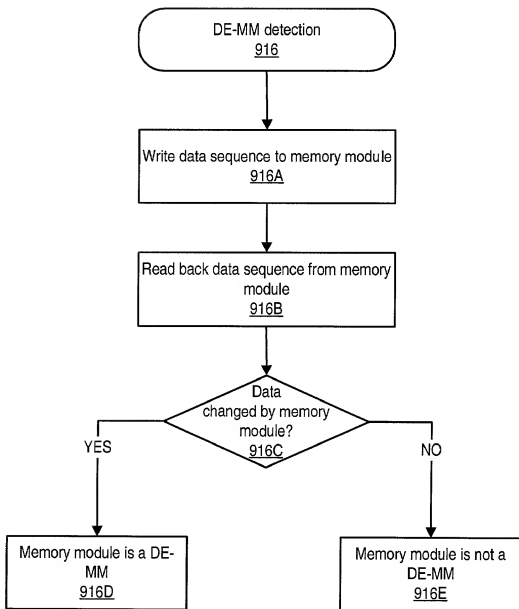


Figure 8

09640724.04301
T06240.12204860

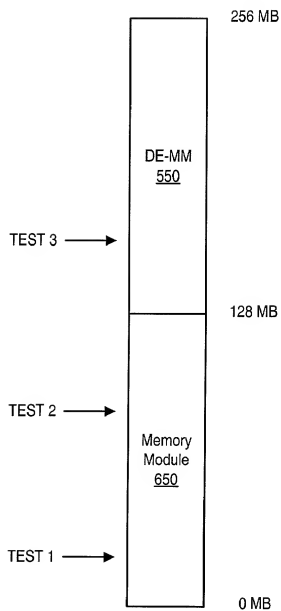


Figure 9

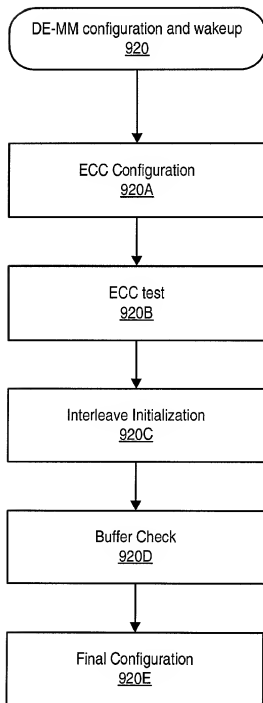


Figure 10

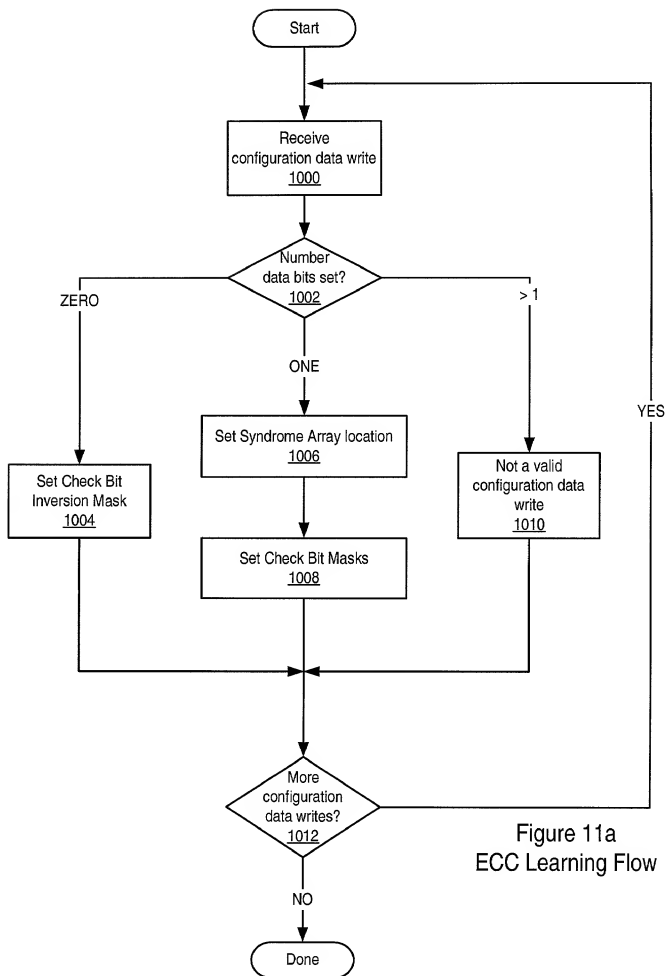


Figure 11a
ECC Learning Flow

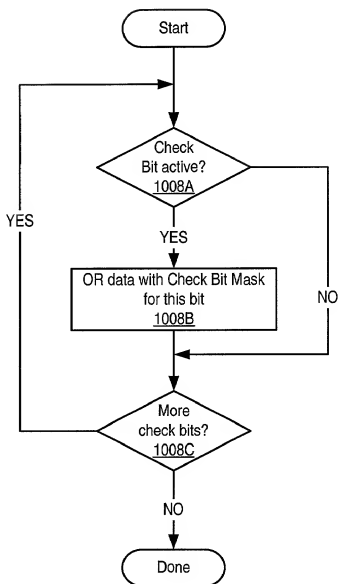


Figure 11b
Learning Check Bit Masks

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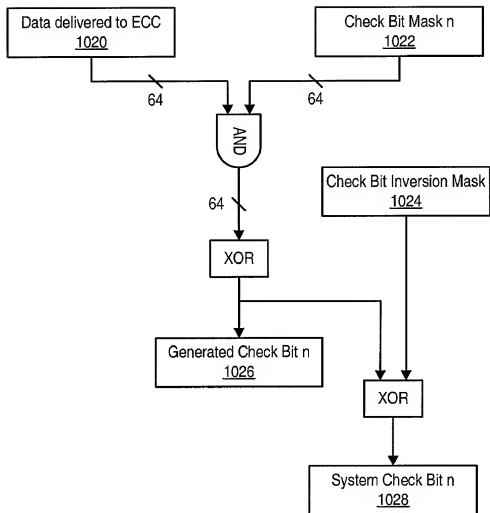


Figure 12
Check Bit Generation

09840724.042301

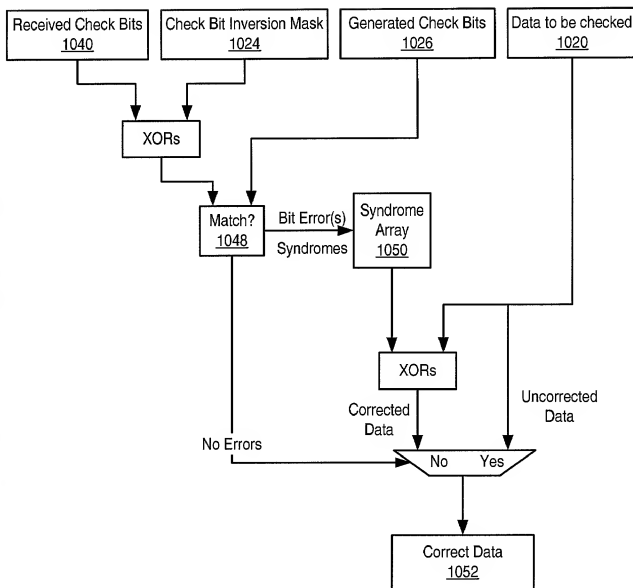


Figure 13
Data Checking and Correction

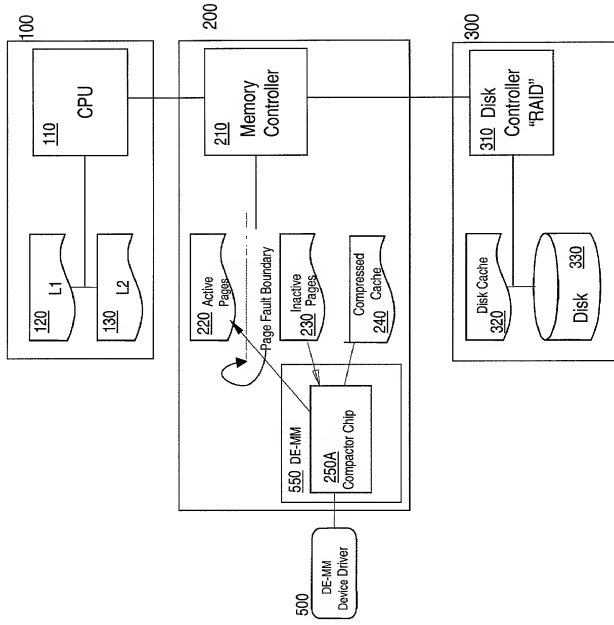


Figure 14

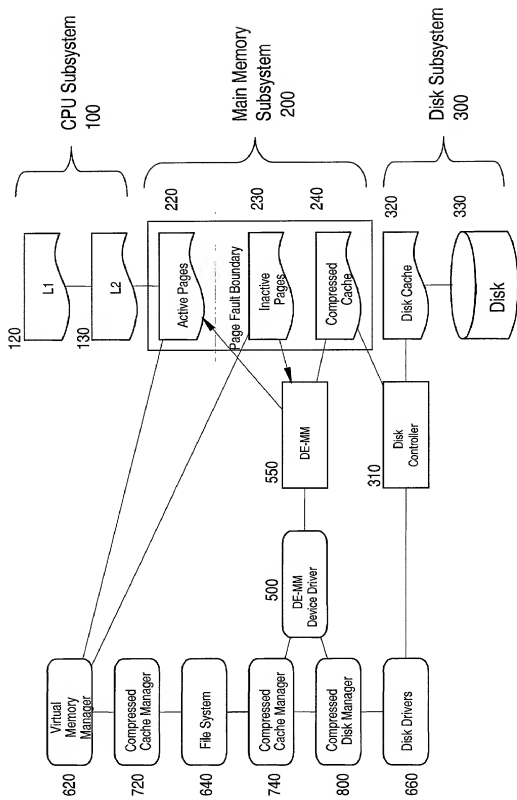


Figure 15